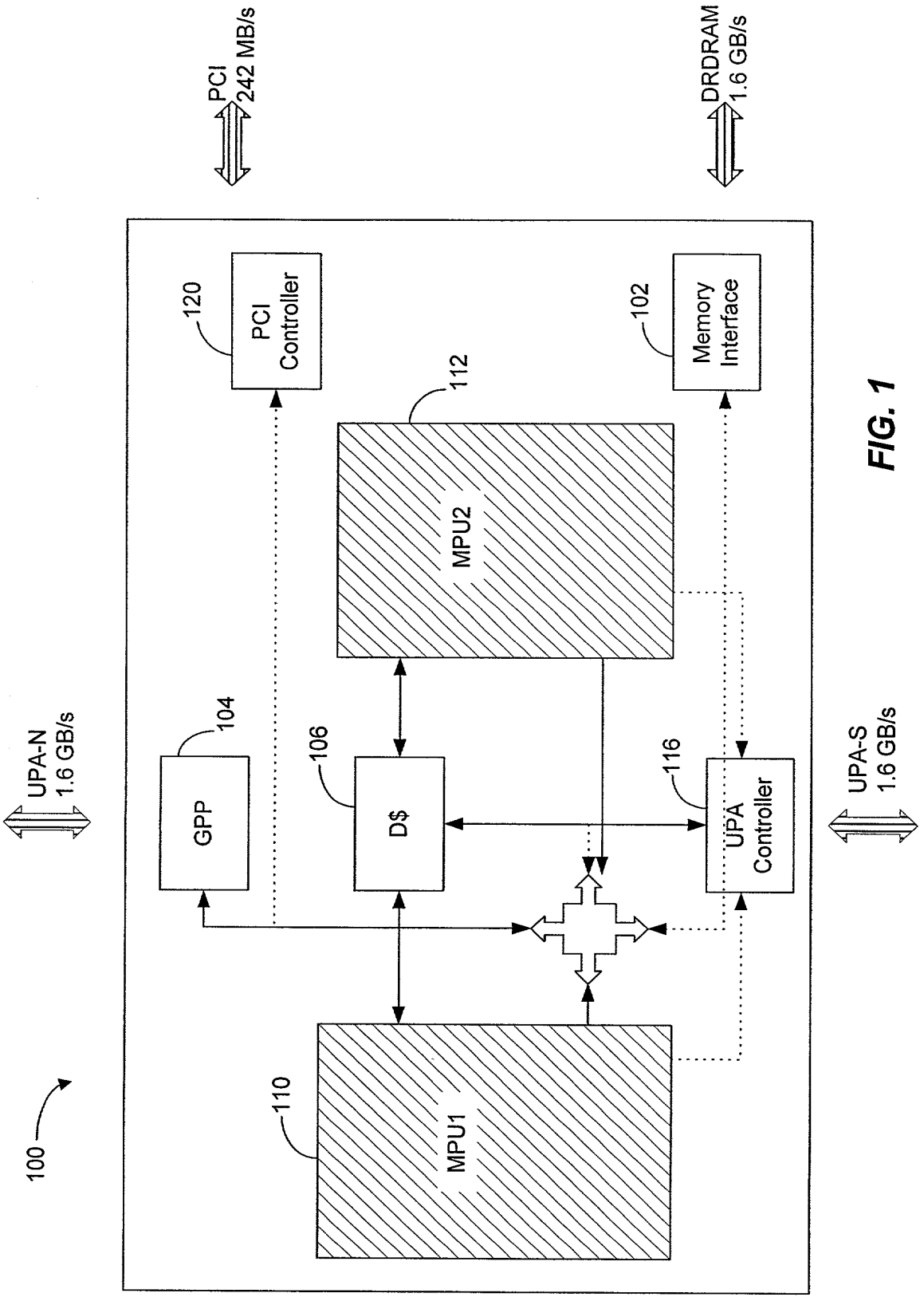
PCI
242 MB/s
DRDRAM
1.6 GB/s
120
PCI Controller
102
Memory Interface
112
MPU2
UPA-N
1.6 GB/s
104
GPP
106
D$
116
UPA Controller
UPA-S
1.6 GB/s
110
MPU1
100

FIG. 1

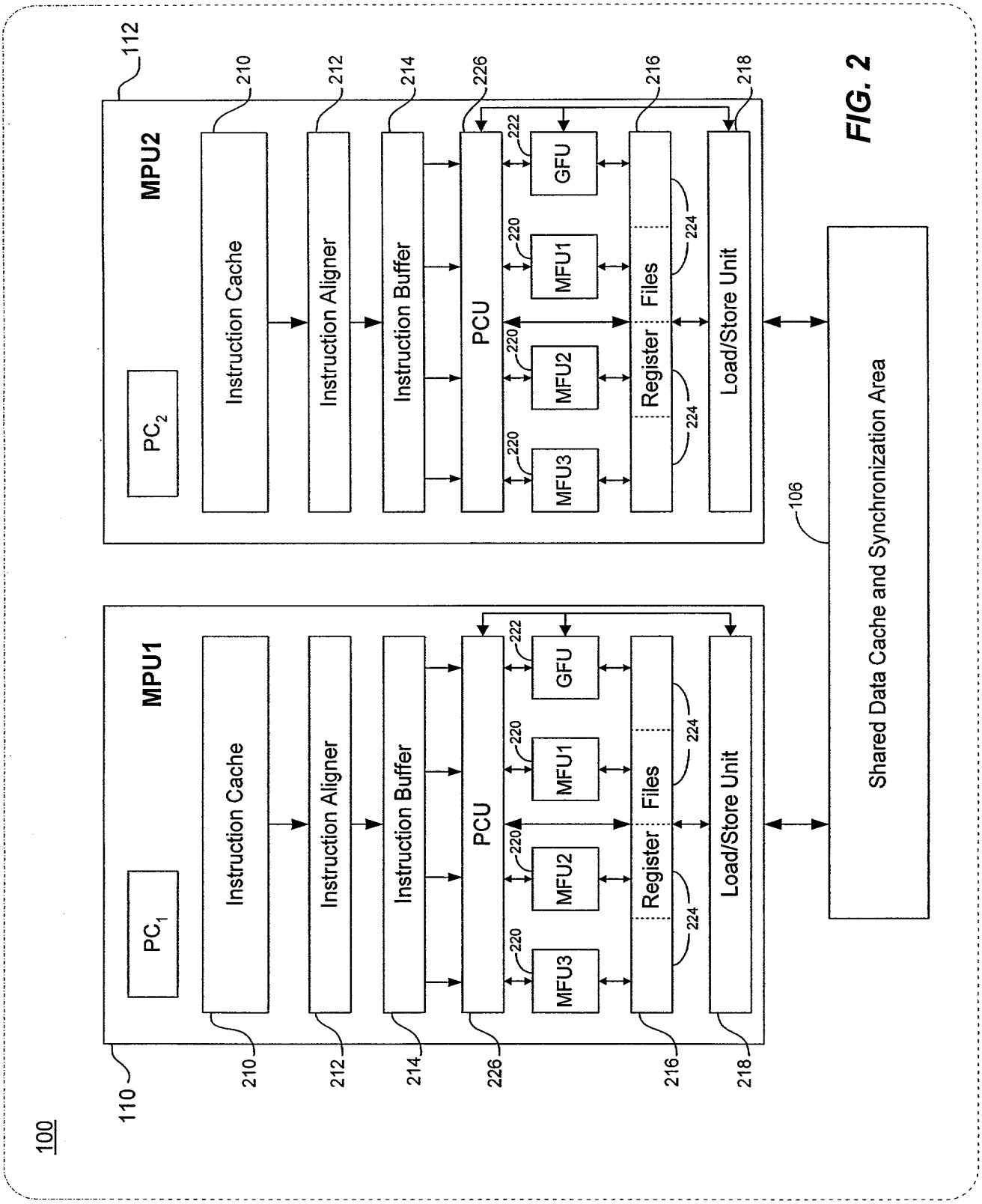
100
MPU1
MPU2
PC1
PC2
Instruction Cache
Instruction Aligner
Instruction Buffer
PCU
GFU
MFU1
MFU2
MFU3
Register Files
Load/Store Unit
Shared Data Cache and Synchronization Area
110
112
210
212
214
216
218
220
222
224
226
106

FIG. 2

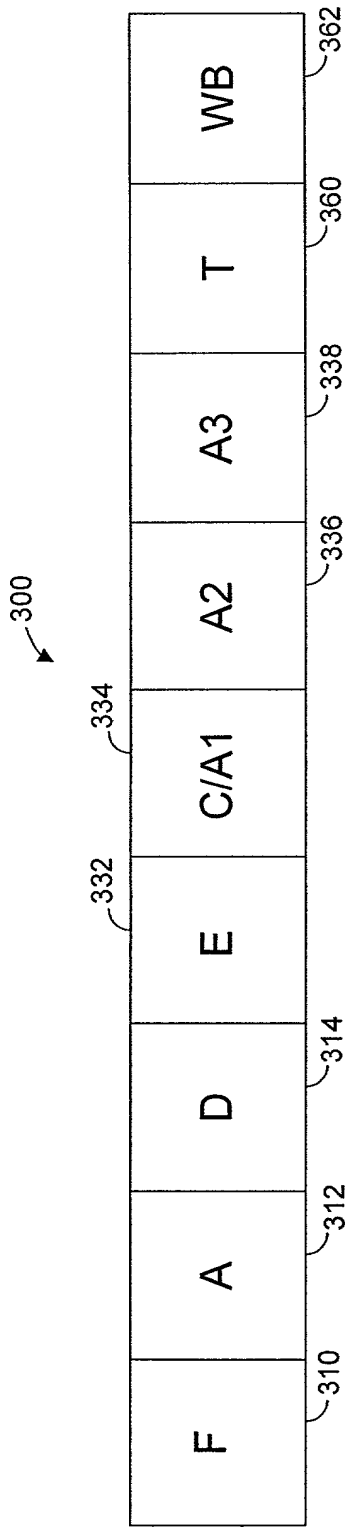

FIG. 3

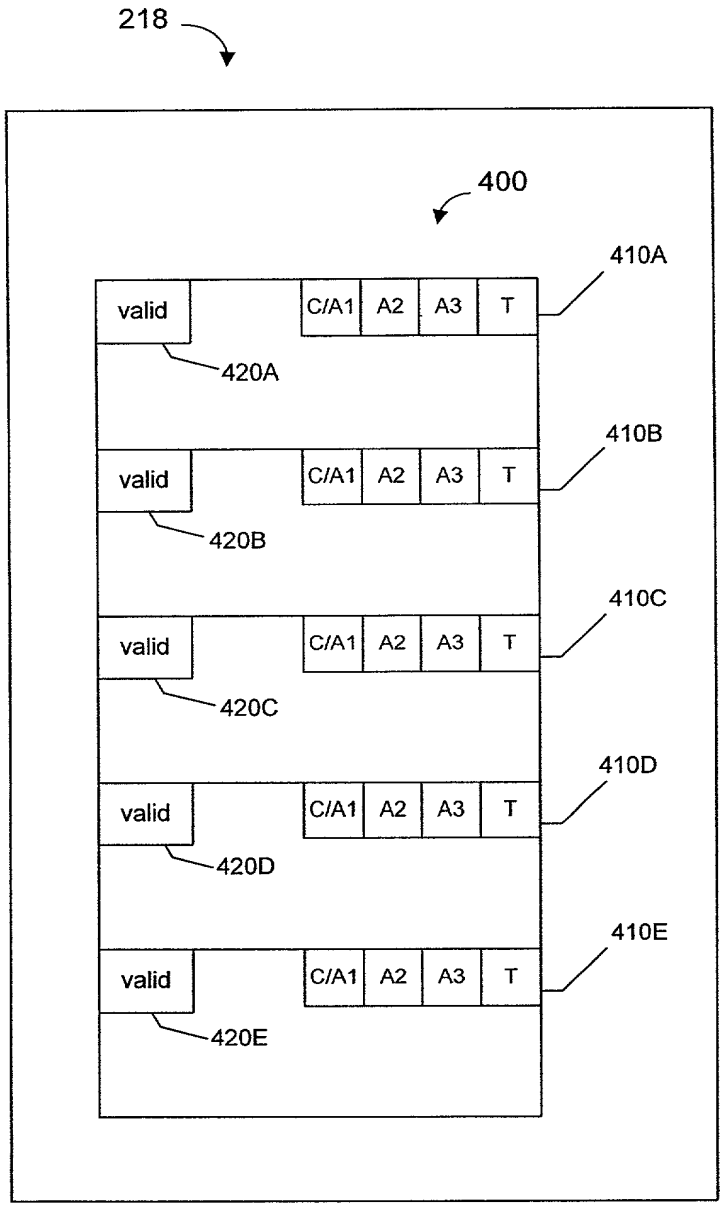
218
400
410A
valid
C/A1
A2
A3
T
420A
410B
valid
C/A1
A2
A3
T
420B
410C
valid
C/A1
A2
A3
T
420C
410D
valid
C/A1
A2
A3
T
420D
410E
valid
C/A1
A2
A3
T
420E

FIG. 4

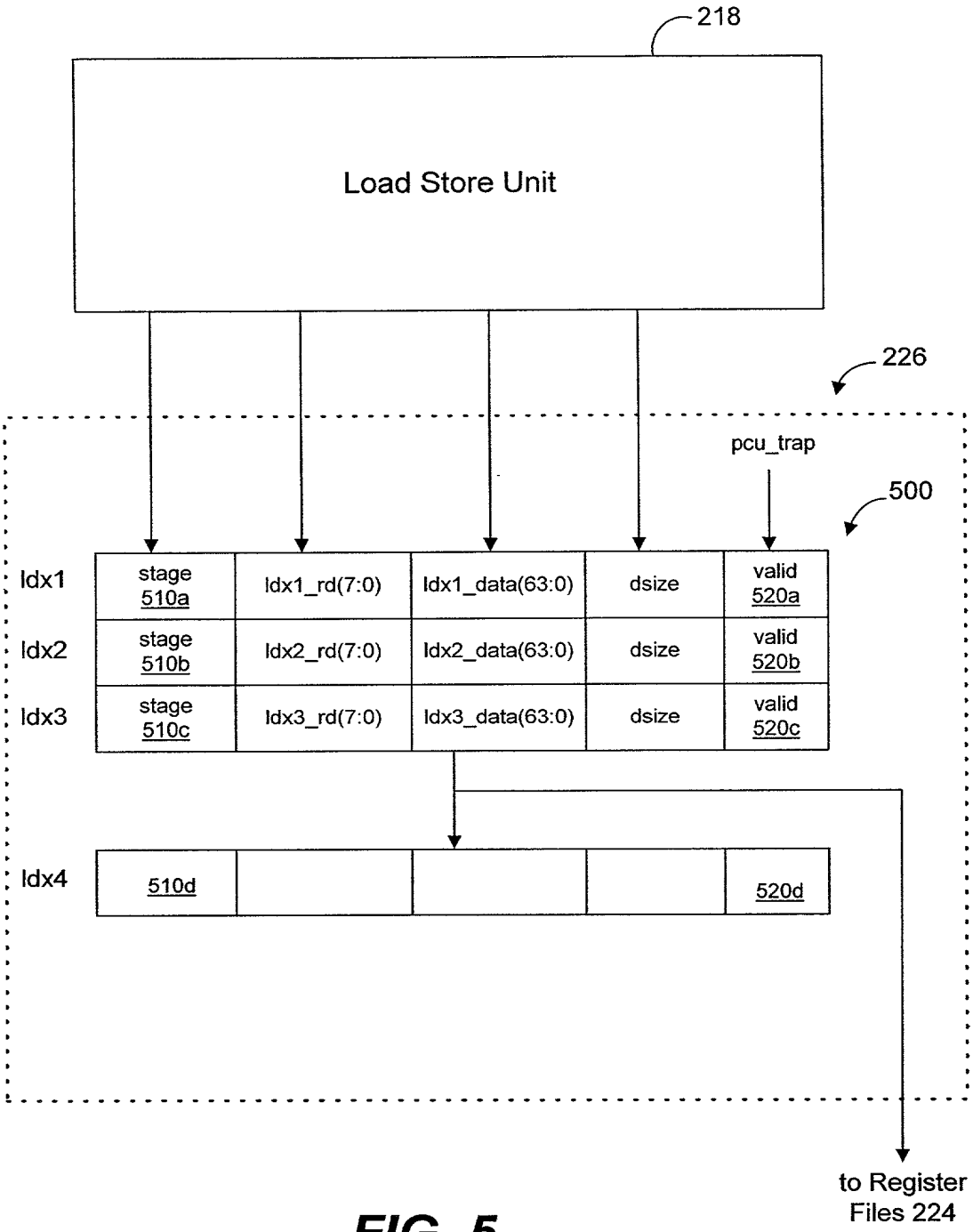
218
Load Store Unit
226
pcu_trap
500
ldx1
stage 510a
ldx1_rd(7:0)
ldx1_data(63:0)
dsize
valid 520a
ldx2
stage 510b
ldx2_rd(7:0)
ldx2_data(63:0)
dsize
valid 520b
ldx3
stage 510c
ldx3_rd(7:0)
ldx3_data(63:0)
dsize
valid 520c
ldx4
510d
520d
to Register Files 224

FIG. 5

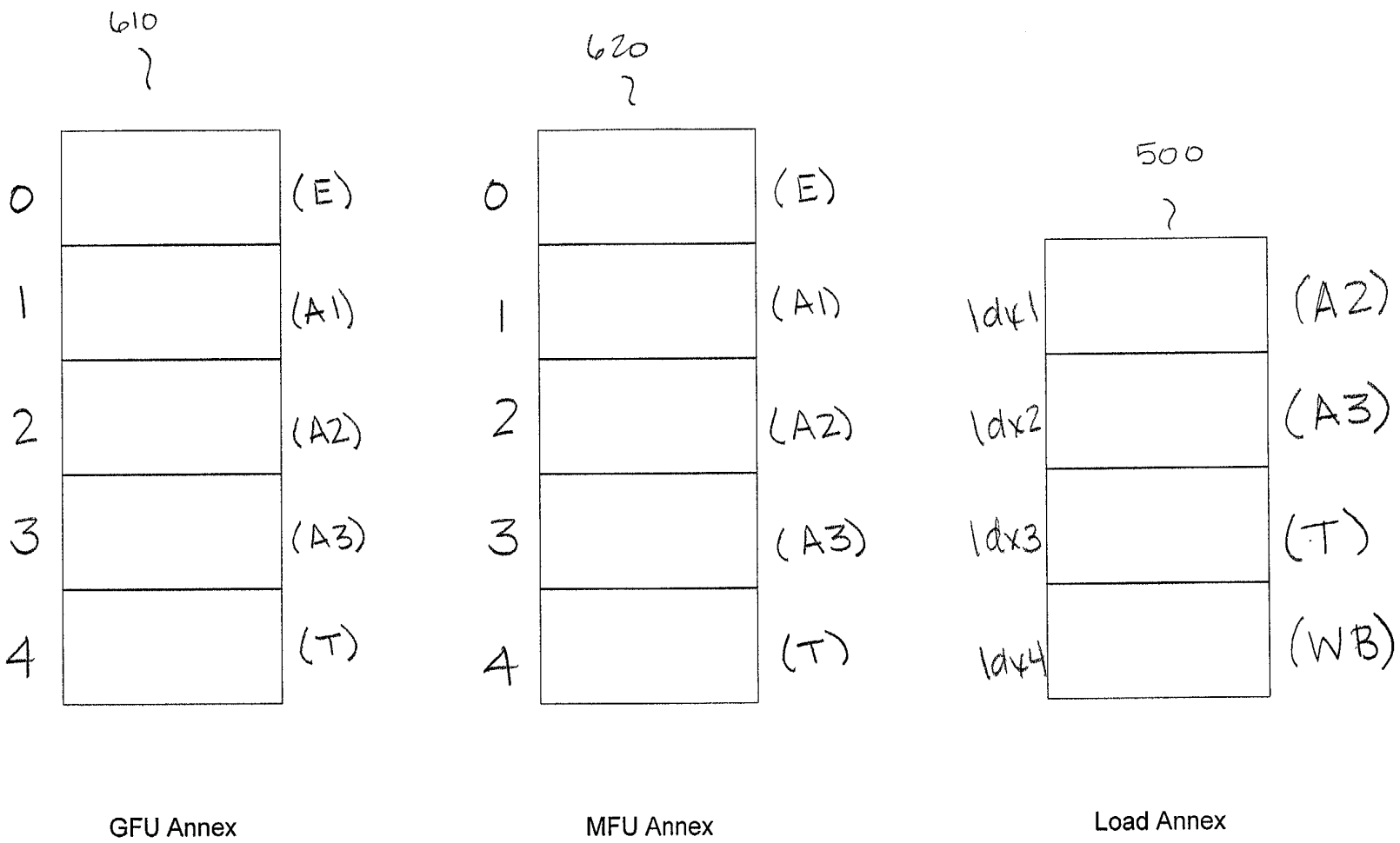
610
0
(E)
1
(A1)
2
(A2)
3
(A3)
4
(T)
GFU Annex
620
0
(E)
1
(A1)
2
(A2)
3
(A3)
4
(T)
MFU Annex
500
ldx1
(A2)
ldx2
(A3)
ldx3
(T)
ldx4
(WB)
Load Annex

FIG. 6

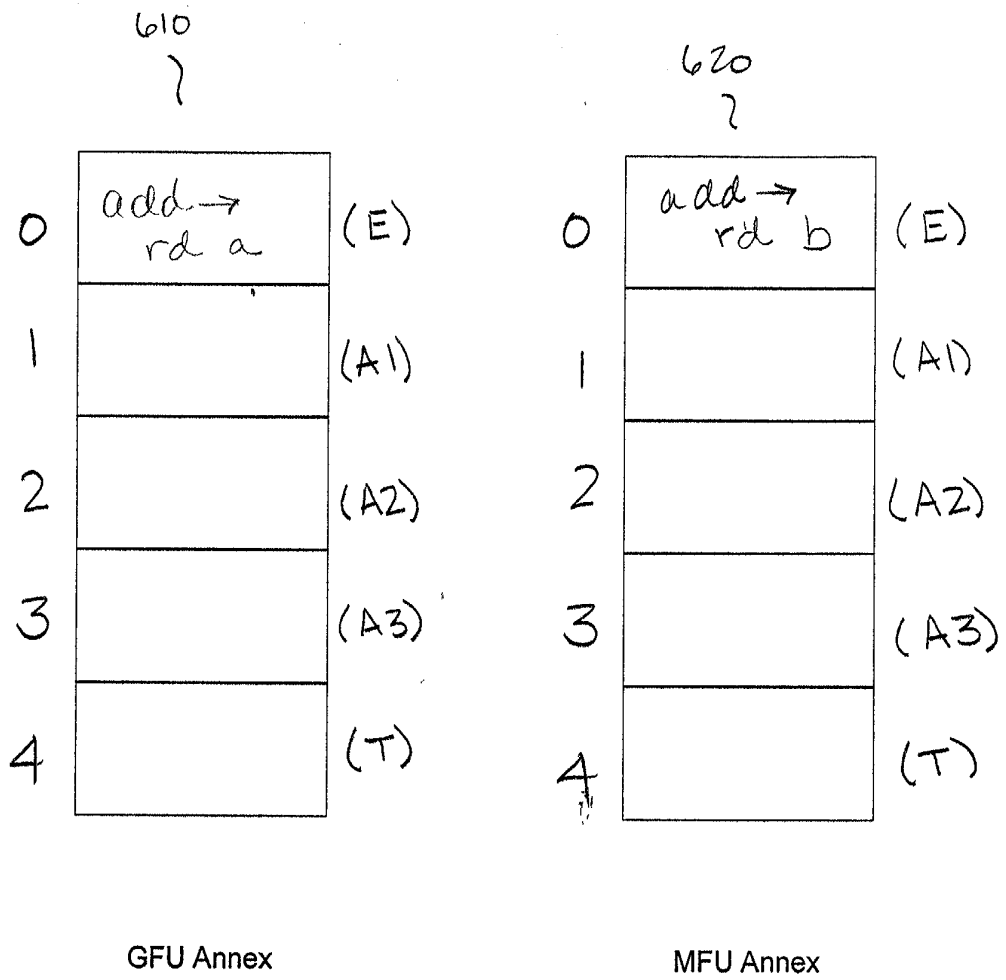

FIG. 6 7

Attorney Docket No.: SP-5106 US
First Inventor: Sharada Yeluri
Title: Forwarding Load Data To Younger Instructions In Annex

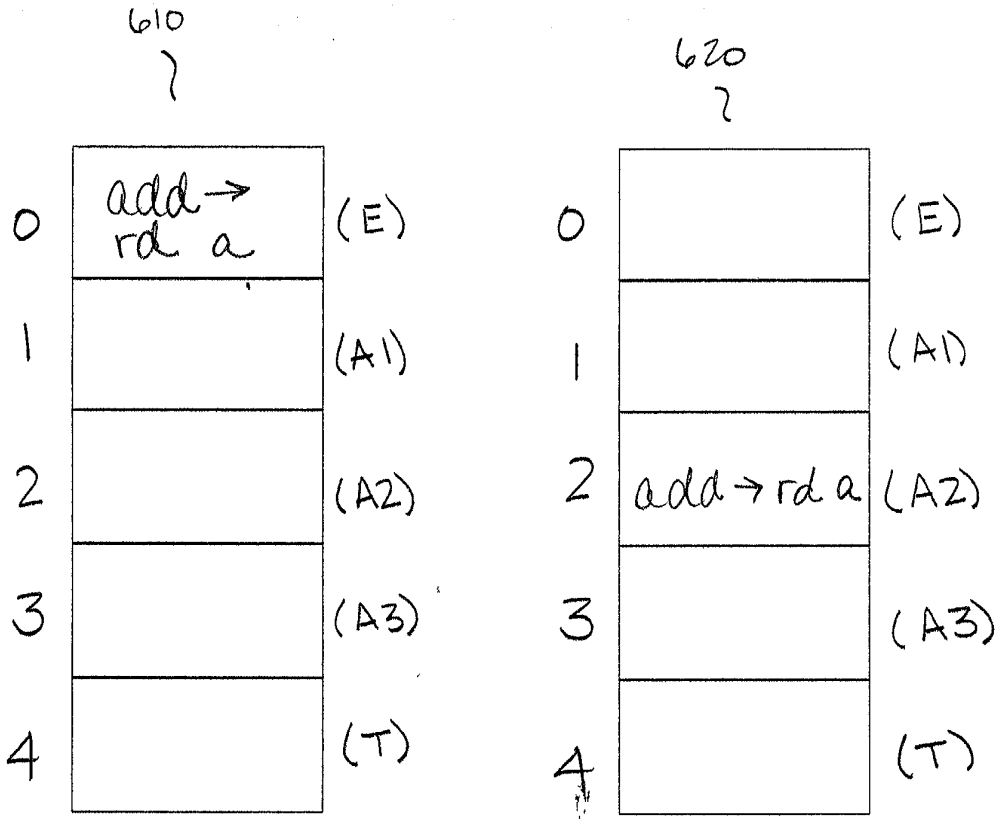

FIG. 8

Attorney Docket No.: SP-5106 US
First Inventor: Sharada Yeluri
Title: Forwarding Load Data To Younger Instructions In Annex

Cycle	1	2	3	4	5	6	7	8	9	10	11	12
(1)	D	E	C/A1	A2 (1dx1)	A3 (1dx2)	T (1dx3)	WB (1dx4)					
(2)		D	D	D	E	A1	A2	A3	T	WB		
(3)					D	E	A1	A2	A3	T	WB	
(4)						D	E	A1	A2	A3	T	WB
(5)							D					

Fig. 9

Attorney Docket No.: SP-5106 US
First Inventor: Sharada Yeluri
Title: Forwarding Load Data To Younger Instructions In Annex

Cycle 4

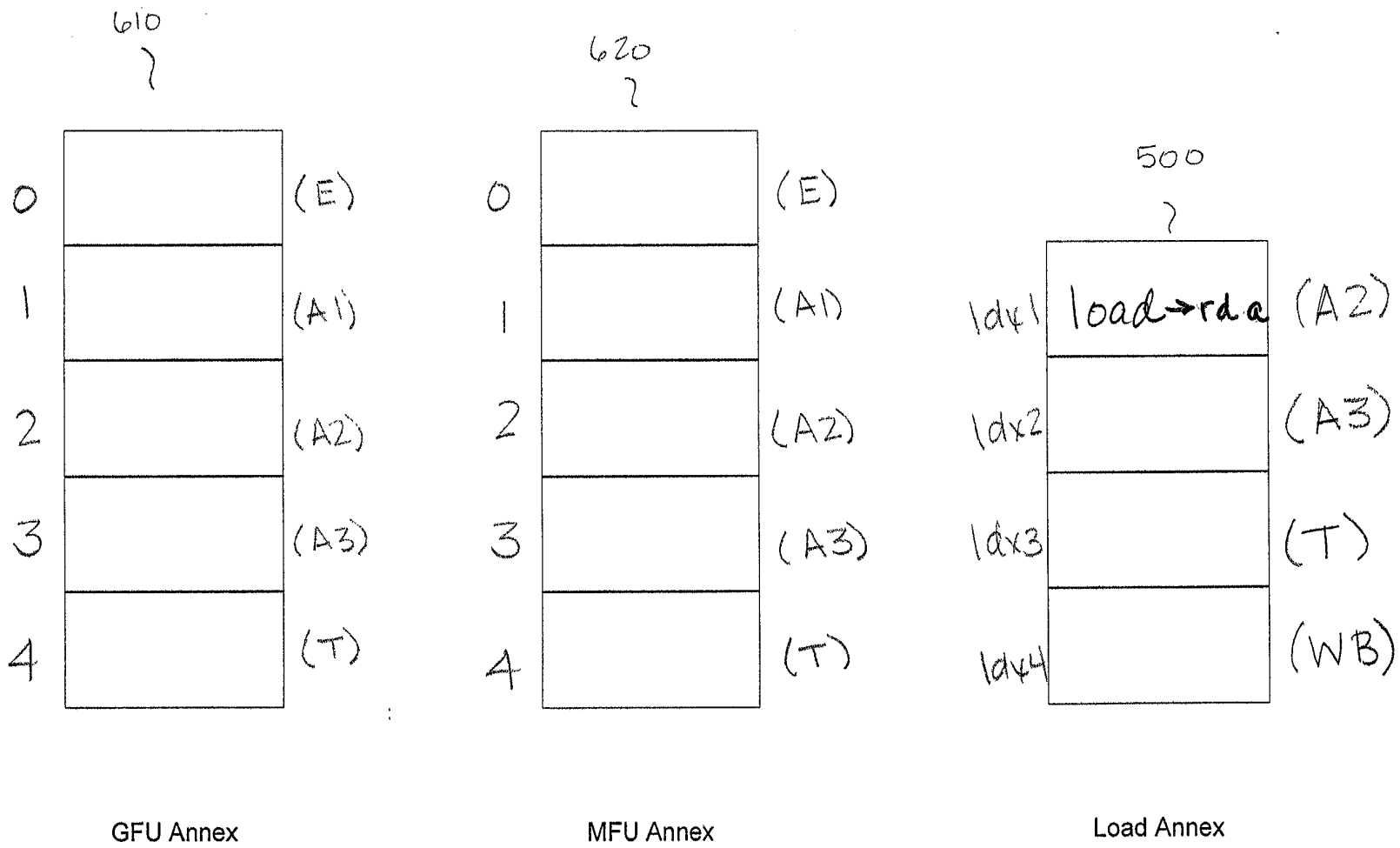

FIG. 6 10

Cycle 5

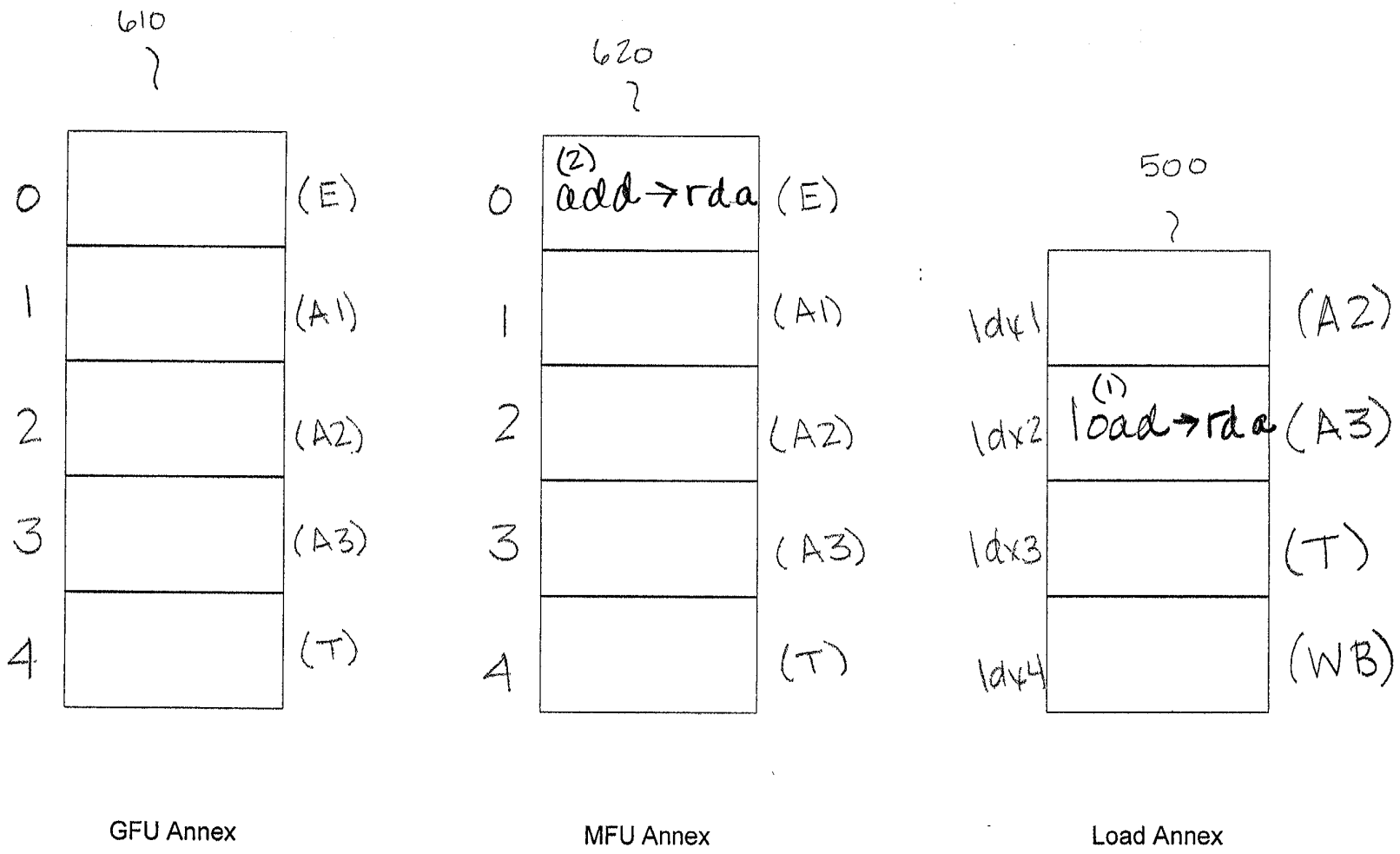

FIG. 6 11

Attorney Docket No.: SP-5106 US
First Inventor: Sharada Yeluri
Title: Forwarding Load Data To Younger Instructions In Annex

Cycle 6

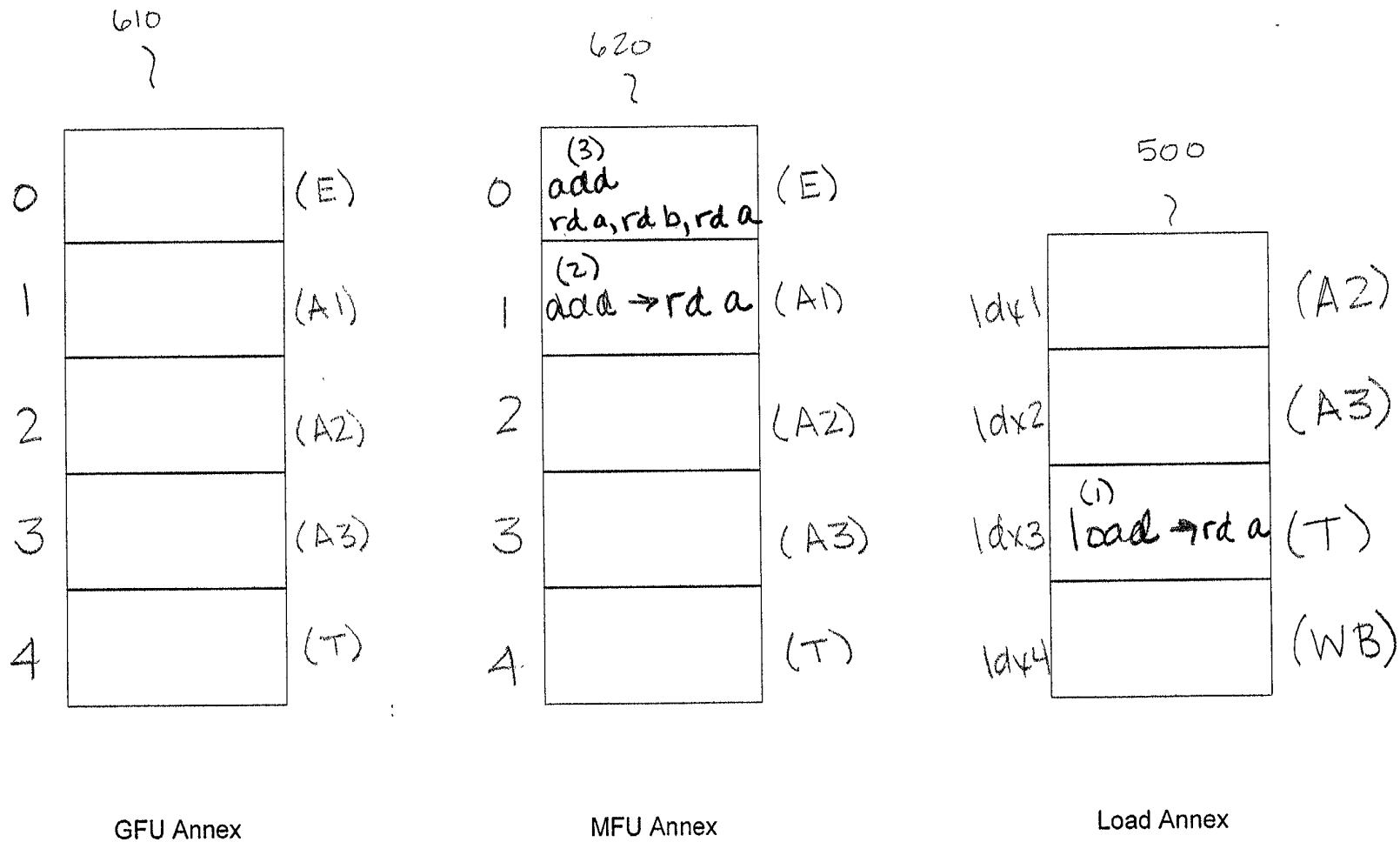

FIG. 6 12

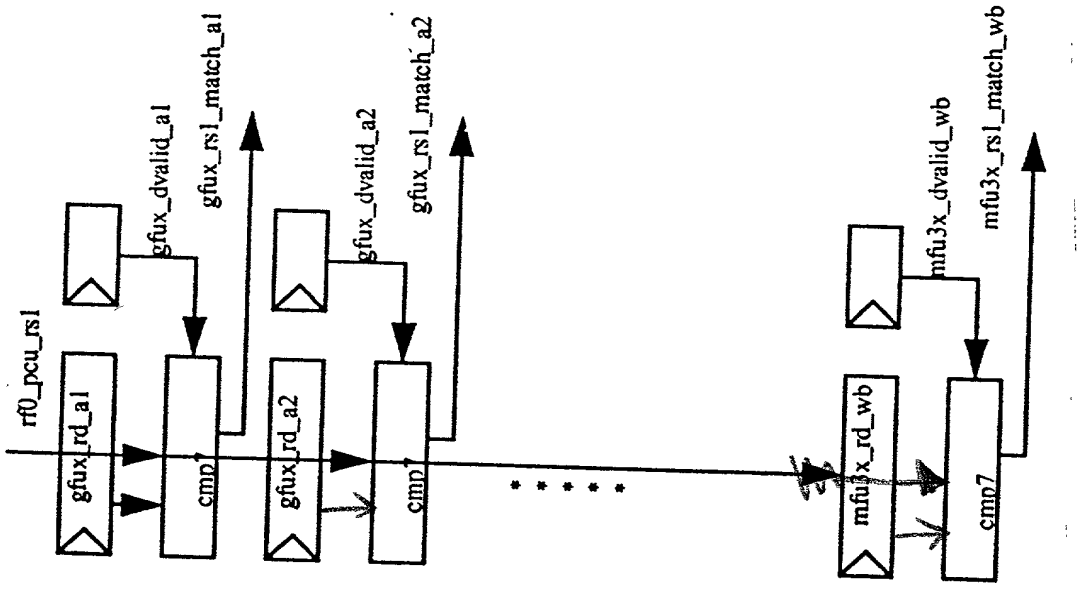
rf0_pcu_rs1
gfux_rd_a1
gfux_dvalid_a1
gfux_rs1_match_a1
cmp1
gfux_rd_a2
gfux_dvalid_a2
gfux_rs1_match_a2
cmp7
mfu3x_rd_wb
mfu3x_dvalid_wb
mfu3x_rs1_match_wb
cmp7

Fig. 13